DATA SHEET

TDA9819
Multistandard vision and sound-IF PLL with DVB-IF processing

Preliminary specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

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Multistandard vision and sound-IF PLL with DVB-IF processing

TDA9819

FEATURES

- 5 V supply voltage
- Applicable for IF frequencies of 38.9 MHz and 45.75 MHz
- Two switched VIF inputs, gain controlled wide band VIF-amplifier (AC-coupled)
- True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics and excellent pulse response)
- VCO frequency switchable between TV (M or BG/L) IF-picture carrier and Digital Video Broadcast (DVB) frequency
- Separate video amplifier for sound trap buffering with high video bandwidth
- VIF AGC detector for gain control, operating as peak sync detector for M and B/G and peak white detector for L; controlled reaction time for L
- Tuner AGC with adjustable takeover point (TOP)
- AFC detector without extra reference circuit
- SIF input for single reference QSS mode (PLL controlled); SIF AGC detector for gain controlled SIF amplifier; single reference QSS mixer able to operate in high performance single reference QSS mode
- AC-coupled limiter amplifier for sound intercarrier signal
- Alignment-free FM-PLL demodulator with high linearity
- AM demodulator without extra reference circuit
- Stabilizer circuit for ripple rejection and to achieve constant output signals.

DVB functions

- Gain controlled IF-amplifier
- Mixer for DVB-IF
- VCO for QAM carrier recovery
- External VCO control for DVB
- Internal and external AGC for DVB
- DVB output level adjust via AGC adjust
- High level DVB operational output amplifier.

GENERAL DESCRIPTION

The TDA9819 is an integrated circuit for multistandard vision and sound-IF signal processing with single reference PLL demodulator combined with the signal stages for DVB-IF processing.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9819	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	5.0	5.5	V
I_P	supply current		81	100	121	mA
$V_{i\ VIF(rms)}$	vision IF input signal voltage sensitivity (RMS value)	−1 dB video at output	–	60	100	μV
$V_{o\ CVBS(p-p)}$	CVBS output signal voltage (peak-to-peak value)		1.7	2.0	2.3	V
B (M, BG/L)	−3 dB video bandwidth on pin 10	M, B/G and L standard; $C_L < 20$ pF; $R_L > 1$ kΩ; AC load	7	8	–	MHz
S/N (W)	weighted signal-to-noise ratio for video		56	60	–	dB
$\alpha_{1.1}$	intermodulation attenuation at 'blue'	f = 1.1 MHz	58	64	–	dB
$\alpha_{3.3}$	intermodulation attenuation at 'blue'	f = 3.3 MHz	58	64	–	dB
α_H	suppression of harmonics in video signal		35	40	–	dB
$V_{i\ SIF(rms)}$	sound-IF input signal voltage sensitivity (RMS value)	−3 dB at intercarrier output	–	70	100	μV
$V_{o(rms)}$	audio output signal voltage for FM (RMS value)	M and B/G standard; 25 kHz frequency deviation	–	0.5	–	V
	audio output signal voltage for AM (RMS value)	L standard; 54% modulation	–	0.5	–	V
THD	total harmonic distortion					
	FM	25 kHz frequency deviation	–	0.15	0.5	%
	AM	54% modulation	–	0.5	1.0	%
S/N (W)	weighted signal-to-noise ratio					
	FM	25 kHz frequency deviation	–	60	–	dB
	AM	54% modulation	47	53	–	dB

BLOCK DIAGRAM

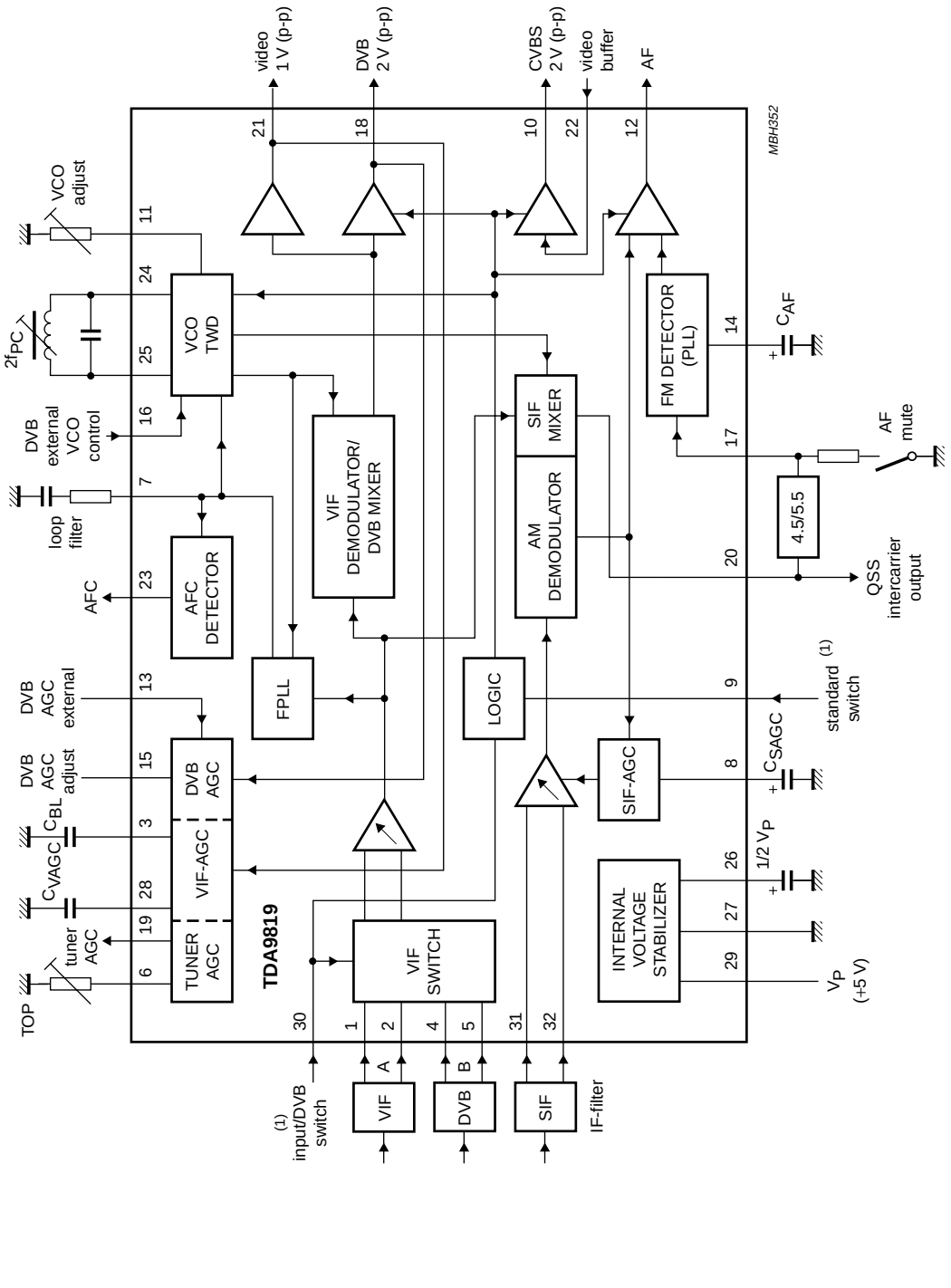


Fig.1 Block diagram.

(1) See switch logic Table 2.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\ VIF1}$	1	VIF differential input signal voltage 1
$V_{i\ VIF2}$	2	VIF differential input signal voltage 2
C_{BL}	3	black level detector
$V_{i\ VIF3}$	4	VIF differential input signal voltage 3
$V_{i\ VIF4}$	5	VIF differential input signal voltage 4
TADJ	6	tuner AGC takeover adjust (TOP)
T_{PLL}	7	PLL loop filter
C_{SAGC}	8	SIF AGC capacitor
STD	9	standard switch input
$V_{o\ CVBS}$	10	2 V CVBS output signal voltage
VCOADJ	11	VCO adjust BG/L/M
$V_{o\ AF}$	12	audio voltage frequency output
$V_{AGC(ext)}$	13	external AGC voltage (DVB)
C_{AF}	14	AF decoupling capacitor
AGCADJ	15	AGC adjust (DVB)
$V_{VCO(ext)}$	16	external VCO control voltage (DVB)
$V_{i\ FM}$	17	sound intercarrier input
DVB	18	DVB output
TAGC	19	tuner AGC output
$V_{o\ QSS}$	20	single reference QSS output voltage
$V_{o(vid)}$	21	composite video output voltage
$V_{i(vid)}$	22	video buffer input voltage
AFC	23	AFC output
VCO1	24	VCO1 reference circuit for $2f_{PC}$
VCO2	25	VCO2 reference circuit for $2f_{PC}$
C_{ref}	26	$\frac{1}{2}V_P$ reference capacitor
GND	27	ground
C_{VAGC}	28	VIF AGC capacitor
V_P	29	supply voltage (+5 V)
INSWI	30	VIF input switch
$V_{i\ SIF1}$	31	SIF differential input signal voltage 1
$V_{i\ SIF2}$	32	SIF differential input signal voltage 2

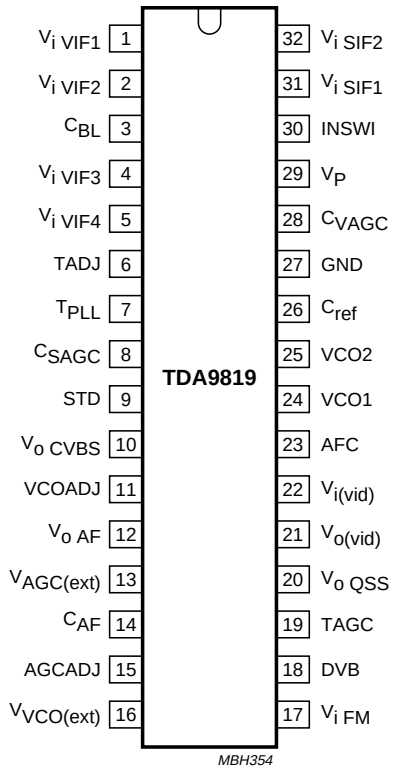


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Vision IF amplifier and input switch

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Each differential stage comprises a feedback network controlled by emitter degeneration to control the IF gain. The first differential stage is extended by two pairs of emitter followers to provide two IF input channels. The VIF input can be selected by pin 30.

Tuner and VIF AGC

The AGC capacitor voltage is transferred to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current (open-collector output).
The tuner AGC takeover point can be adjusted.
This allows the tuner and the SWIF filter to be matched to achieve the optimum IF input level.

The AGC detector charges/discharges the AGC capacitor to the required voltage for setting of VIF and tuner gain in order to keep the video signal at a constant level. Therefore for negative video modulation the sync level and for positive video modulation the peak white level of the video signal is detected. In order to reduce the reaction time for positive modulation, where a very large time constant is needed, an additional level detector increases the discharging current of the AGC capacitor (fast mode) in the event of a decreasing VIF amplitude step.
The additional level information is given by the black-level detector voltage.

Frequency Phase Locked Loop detector (FPLL)

The VIF-amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier. During acquisition the frequency detector produces a DC current proportional to the frequency difference between the input and the VCO signal. After frequency lock-in the phase detector produces a DC current proportional to the phase difference between the VCO and the input signal. The DC current of either frequency detector or phase detector is converted into a DC voltage via the loop filter, which controls the VCO frequency. In the event of positive modulated signals the phase detector is gated by composite sync in order to avoid signal distortion for overmodulated VIF signals.

VCO, Travelling Wave Divider (TWD) and AFC

The VCO operates with a resonance circuit (with L and C in parallel) at double the PC frequency. The VCO is controlled by two integrated variable capacitors.
The control voltage required to tune the VCO from its free-running frequency to actually double the PC frequency is generated by the frequency-phase detector and fed via the loop filter to the first variable capacitor (FPLL). This control voltage is amplified and converted into a current which represents the AFC output signal. The VCO centre frequency can be decreased by activating an additional internal capacitor. With a variable resistor at VCOADJ (pin 11) the frequency for the M, B/G and L mode can be tuned to the picture carrier frequency. At centre frequency the AFC output current is equal to zero.

The oscillator signal is divided-by-two with a TWD which generates two differential output signals with a 90 degree phase difference independent of the frequency.

Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The vision IF input signal is multiplied with the ‘in phase’ signal of the travelling wave divider output. In the demodulator stage the video signal polarity can be switched in accordance with the TV standard.

The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the video amplifier. The video amplifier is realized by an operational amplifier with internal feedback and high bandwidth. A low-pass filter is integrated to achieve an attenuation of the carrier harmonics for M, B/G and L standard. The standard dependent level shift in this stage delivers the same sync level for positive and negative modulation. The video output signal is 1 V (p-p) for nominal vision IF modulation.

Video buffer

For an easy adaption of the sound traps an operational amplifier with internal feedback is used in the event of M, B/G and L standard. This amplifier is featured with a high bandwidth and 7 dB gain. The input impedance is adapted for operating in combination with ceramic sound traps. The output stage delivers a nominal 2 V (p-p) positive video signal. Noise clipping is provided.

SIF amplifier and AGC

The sound IF amplifier consists of two AC-coupled differential amplifier stages. Each differential stage comprises a controlled feedback network provided by emitter degeneration.

The SIF AGC detector is related to the SIF input signals (average level of AM or FM carriers) and controls the SIF amplifier to provide a constant SIF signal to the AM demodulator and single reference QSS mixer. The SIF AGC reaction time is set to ‘slow’ for nominal video conditions. But with a decreasing VIF amplitude step the SIF AGC is set to ‘fast’ mode controlled by the VIF AGC detector. In FM mode this reaction time is also set to ‘fast’ controlled by the standard switch.

Single reference QSS mixer

The single reference QSS mixer is realized by a multiplier. The SIF amplifier output signal is fed to the single reference QSS mixer and converted to intercarrier frequency by the regenerated picture carrier (VCO). The mixer output signal is fed via a high-pass for attenuation of the video signal components to the output pin 20. With this system a high performance hi-fi stereo sound processing can be achieved.

For a simplified application without a sound-IF SAW filter the single reference QSS mixer can be switched to the intercarrier mode by connecting pins 31 and 32 to ground (see note 18 of Chapter “Characteristics”).

In this mode the sound-IF passes the VIF SAW filter and the composite IF signal is fed to the single reference QSS mixer. This IF signal is multiplied by the 90° TWD output signal for converting the sound-IF to intercarrier frequency. By using this quadrature detection, the low frequency video signals are removed.

Due to the sound-IF attenuation in the VIF filter (sound shelf), the audio signal-to-noise (S/N) figure decreases.

AM demodulator

The AM demodulator (French L standard) is realized by a multiplier. The modulated SIF amplifier output signal is multiplied in phase with the limited (AM is removed) SIF amplifier output signal. The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the AF amplifier.

FM detector

The FM detector consists of a limiter, an FM-PLL and an AF amplifier. The limiter provides the amplification and limitation of the FM sound intercarrier signal before demodulation. The result is high sensitivity and AM suppression. The amplifier consists of 7 stages which are internally AC-coupled in order to minimize the DC offset and to save pins for DC decoupling.

The FM-PLL consists of an integrated relaxation oscillator, an integrated loop filter and a phase detector.
The oscillator is locked to the FM intercarrier signal, output from the limiter. As a result of locking, the oscillator frequency tracks with the modulation of the input signal and the oscillator control voltage is superimposed by the AF voltage. The FM-PLL operates as an FM-demodulator.

The AF amplifier consists of two parts:

1. The AF preamplifier for FM sound is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF voltage from the PLL demodulator, by principle a small output signal, is amplified by approximately 30 dB. The low-pass characteristic of the amplifier reduces the harmonics of the intercarrier signal at the sound output terminal. An additional DC control circuit is implemented to keep the DC level constant, independent of process spread.
2. The AF output amplifier (10 dB) provides the required output level by a rail-to-rail output stage. This amplifier makes use of an input selector for switching to AM/FM or mute state, controlled by the standard switching voltage and the mute switching voltage.

Internal voltage stabilizer and $\frac{1}{2}V_P$ reference

The band-gap circuit internally generates a voltage of approximately 1.25 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.6 V which is used as an internal reference voltage.

For all audio output signals the constant reference voltage cannot be used because large output signals are required. Therefore these signals refer to half the supply voltage to achieve a symmetrical headroom, especially for the rail-to-rail output stage. For ripple and noise attenuation the $\frac{1}{2}V_P$ voltage has to be filtered via a low-pass filter by using an external capacitor together with an integrated resistor (f_g = 5 Hz). For a fast setting to $\frac{1}{2}V_P$ an internal start-up circuit is added.

DVB mixer

The VCO can be controlled by an external DC signal to provide a carrier for the down-conversion of the DVB-IF signal. The VCO frequency as a function of the voltage at pin 16 is given in Figs 10 and 11.

DVB AGC

For the DVB operation a peak AGC detector is activated. The peak value of (digital) QAM signal is detected and controlled to a constant value by the variable VIF amplifier. The detector bandwidth is adapted to the signal frequency (3 to 11 MHz). The external AGC time constant is given by the VIF AGC capacitor at pin 28.

The DVB output signal $V_{O\ DVB}$ can be adjusted in a range of ±3 dB by a control voltage ΔV_{adj} at pin 15. The internal AGC can be switched off (see Table 2) and the IF gain can be controlled by an external voltage at pin 13. The tuner AGC is active in both instances.

DVB output buffer

The output buffer for the DVB signal has a high bandwidth and 0 dB gain. An inverting configuration was chosen to obtain minimum distortion. For non-DVB standards the buffer is switched to a mute to reduce the output signal level.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage (pin 29)	maximum chip temperature of 125 °C; note 1	0	7.0	V
V_n	voltage at pins 1 to 9, 11 to 13, 15, 16, 19, 22, 23 and 28 to 32		0	V_P	V
$t_{sc(max)}$	maximum short-circuit time		–	10	s
V_{19}	tuner AGC output voltage		0	13.2	V
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		–20	+70	°C
V_{es}	electrostatic handling voltage	note 2	–300	+300	V

Notes

1. I_P = 125 mA; T_{amb} = 70 °C; $R_{th\ j\text{-}a}$ = 60 K/W.
2. Machine model class B.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	60	K/W

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; see Table 1 for input frequencies and level; input level $V_{i\ IF1-2,\ 4-5}$ = 10 mV RMS value (sync-level for M and B/G, peak white level for L); video modulation DSB; residual carrier M and B/G: 10%; L = 3%; video signal in accordance with "*CCIR, line 17*"; measurements taken in Fig.12; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 29)						
V_P	supply voltage	note 1	4.5	5.0	5.5	V
I_P	supply current	M, B/G and L standard	89	105	121	mA
		DVB	81	96	111	mA
Vision IF amplifier (pins 1, 2, 4 and 5)						
$V_{i\ VIF(rms)}$	input signal voltage sensitivity (RMS value)	M, B/G and L standard; −1 dB video at output	–	60	90	μV
$V_{i\ max(rms)}$	maximum input signal voltage (RMS value)	M, B/G and L standard; +1 dB video at output	140	200	–	mV
$\Delta V_{o(int)}$	internal IF amplitude difference between picture and sound carrier	within AGC range; Δf = 5 MHz	–	0.7	1	dB
G_{IF}	IF gain control range	see Fig.3	65	70	–	dB
$R_{i(diff)}$	differential input resistance	note 2; input activated	1.7	2.2	2.7	kΩ
$C_{i(diff)}$	differential input capacitance	note 2; input activated	1.2	1.7	2.5	pF
$V_{1, 2, 4, 5}$	DC input voltage	note 2; input activated	–	3.3	–	V
R_i	input resistance to ground	note 2; input not activated	–	1.1	–	kΩ
$V_{1, 2, 4, 5}$	DC input voltage	note 2; input not activated	–	0.2	–	V
$\alpha_{i\ IF}$	crosstalk attenuation of IF input switch at pins 1, 2, 4 and 5	notes 2 and 3	55	60	–	dB
True synchronous video demodulator; note 4						
$f_{VCO(max)}$	maximum oscillator frequency for carrier regeneration	$f = 2f_{PC}$	125	130	–	MHz
$\frac{\Delta f_{osc}}{\Delta T}$	oscillator drift as a function of temperature	free-running oscillator; I_{AFC} = 0; note 5	–	–	±20	ppm/K
$V_{0\ ref(rms)}$	oscillator voltage swing between pins 24 and 25 (RMS value)		–	60	–	mV
$f_{PC\ CR}$	vision carrier capture range	M standard	±1.0	±1.25	–	MHz
		B/G and L standard	±1.35	±1.6	–	MHz
$\Delta f_{PC(fr)}$	vision carrier frequency accuracy (free-running)	M standard	–	±150	±300	kHz
		B/G and L standard	–	±200	±400	kHz
$\Delta f_{PC(alg)}$	frequency alignment range	I_{AFC} = 0; M standard	±300	±400	–	kHz
		I_{AFC} = 0; B/G and L standard	±400	±600	–	kHz
t_{acq}	acquisition time	BL = 70 kHz; note 6	–	–	30	ms
$V_{i\ VIF(rms)}$	VIF input signal voltage sensitivity for PLL to be locked (RMS value; pins 1, 2, 4 and 5)	maximum IF gain; note 7	–	60	90	μV
$I_{FPLL(offset)}$	FPLL offset current at pin 7	note 8	–	–	±4.5	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Composite video amplifier (pin 21; sound carrier off)						
$V_{o\ video(p-p)}$	output signal voltage (peak-to-peak value)	see Fig.8	0.88	1.0	1.12	V
$V_{21(sync)}$	sync voltage level		–	1.5	–	V
$V_{21(clu)}$	upper video clipping voltage level		$V_P - 1.1$	$V_P - 1$	–	V
$V_{21(cll)}$	lower video clipping voltage level		–	0.7	0.9	V
$R_{o,21}$	output resistance	note 2	–	–	10	Ω
$I_{int\ 21}$	internal DC bias current for emitter-follower		1.6	2.0	–	mA
$I_{21\ max(sink)}$	maximum AC and DC output sink current		1.0	–	–	mA
$I_{21\ max(source)}$	maximum AC and DC output source current		2.0	–	–	mA
B_{-1}	−1 dB video bandwidth	$C_L < 50$ pF; $R_L > 1$ kΩ; AC load	5	6	–	MHz
B_{-3}	−3 dB video bandwidth	$C_L < 50$ pF; $R_L > 1$ kΩ; AC load	7	8	–	MHz
α_H	suppression of video signal harmonics	$C_L < 50$ pF; $R_L > 1$ kΩ; AC load; note 9	35	40	–	dB
PSRR	power supply ripple rejection at pin 21	video signal; grey level; see Fig.9				
		M and B/G standard	32	35	–	dB
		L standard	26	30	–	dB
CVBS buffer amplifier (only) and noise clipper (pins 10 and 22)						
$R_{i,22}$	input resistance	note 2	2.6	3.3	4.0	kΩ
$C_{i,22}$	input capacitance	note 2	1.4	2	3.0	pF
$V_{I,22}$	DC input voltage		1.5	1.8	2.1	V
G_v	voltage gain	M, B/G and L standard; note 10	6.5	7	7.5	dB
$V_{10(clu)}$	upper video clipping voltage level		3.9	4.0	–	V
$V_{10(cll)}$	lower video clipping voltage level		–	1.0	1.1	V
$R_{o,10}$	output resistance	note 2	–	–	10	Ω
$I_{int\ 10}$	DC internal bias current for emitter-follower		2.0	2.5	–	mA
$I_{o,10\ max(sink)}$	maximum AC and DC output sink current		1.4	–	–	mA
$I_{o,10\ max(source)}$	maximum AC and DC output source current		2.4	–	–	mA
B_{-1}	−1 dB video bandwidth	$C_L < 20$ pF; $R_L > 1$ kΩ; AC load	8.4	11	–	MHz
B_{-3}	−3 dB video bandwidth	$C_L < 20$ pF; $R_L > 1$ kΩ; AC load	11	14	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Measurements from IF input to CVBS output (pin 10; 330 Ω between pins 21 and 22, sound carrier off)						
$V_{o\ CVBS(p-p)}$	CVBS output signal voltage on pin 10 (peak-to-peak value)	note 10	1.7	2.0	2.3	V
$V_{o\ CVBS(sync)}$	sync voltage level	M and B/G standard	–	1.35	–	V
		L standard	–	1.35	–	V
ΔV_o	deviation of CVBS output signal voltage at M and B/G standard	50 dB gain control	–	–	0.5	dB
		30 dB gain control	–	–	0.1	dB
$\Delta V_{o(blBG)}$	black level tilt in M and B/G standard	gain variation; note 11	–	–	1	%
$\Delta V_{o(blL)}$	black level tilt for worst case in L standard	vision carrier modulated by test line (VITS) only; gain variation; note 11	–	–	1.9	%
G_{diff}	differential gain	*"CCIR, line 330"*	–	2	5	%
φ_{diff}	differential phase	*"CCIR, line 330"*	–	1	2	deg
B_{-1}	–1 dB video bandwidth	C_L < 20 pF; R_L > 1 kΩ; AC load; M, B/G and L standard	5	6	–	MHz
B_{-3}	–3 dB video bandwidth	C_L < 20 pF; R_L > 1 kΩ; AC load; M, B/G and L standard	7	8	–	MHz
S/N (W)	weighted signal-to-noise ratio	see Fig.5 and note 12	56	60	–	dB
S/N	unweighted signal-to-noise ratio	see Fig.5 and note 12	49	53	–	dB
$IM\alpha_{1.1}$	intermodulation attenuation at 'blue'	f = 1.1 MHz; see Fig.6 and note 13	58	64	–	dB
	intermodulation attenuation at 'yellow'	f = 1.1 MHz; see Fig.6 and note 13	60	66	–	dB
$IM\alpha_{3.3}$	intermodulation attenuation at 'blue'	f = 3.3 MHz; see Fig.6 and note 13	58	64	–	dB
	intermodulation attenuation at 'yellow'	f = 3.3 MHz; see Fig.6 and note 13	59	65	–	dB
$\alpha_{c(rms)}$	residual vision carrier (RMS value)	fundamental wave and harmonics; M, B/G and L standard	–	2	10	mV
$\alpha_{H(sup)}$	suppression of video signal harmonics	note 9	35	40	–	dB
$\alpha_{H(spur)}$	spurious elements	note 14	40	–	–	dB
PSRR	power supply ripple rejection at pin 10	video signal; grey level; see Fig.9				
		M and B/G standard	25	28	–	dB
		L standard	20	23	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIF-AGC detector (pin 28)						
I_{28}	charging current	M, B/G and L standard; note 11	0.75	1	1.25	mA
	additional charging current	L standard in event of missing VITS pulses and no white video content	1.9	2.5	3.1	μA
	discharging current	M and B/G standard	15	20	25	μA
		normal mode L	225	300	375	nA
		fast mode L	30	40	50	μA
t_{resp}	AGC response to an increasing VIF step	M, B/G and L standard; note 15	–	–	0.1	ms/dB
	AGC response to a decreasing VIF step	M and B/G standard	–	2.2	3.5	ms/dB
		fast mode L	–	1.1	1.8	ms/dB
		normal mode L; note 15	–	150	240	ms/dB
ΔIF	VIF amplitude step for activating fast AGC mode	L standard	–2	–6	–10	dB
$V_{3(th)}$	threshold voltage level additional charging current	see Fig.8				
		L standard	–	1.95	–	V
		L standard; fast mode L	–	1.65	–	V
Tuner AGC (pin 19)						
$V_{i(rms)}$	IF input signal voltage for minimum starting point of tuner takeover (RMS value)	input at pins 1, 2, 4 and 5; R_{TOP} = 22 kΩ; I_{19} = 0.4 mA	–	2	5	mV
	IF input signal voltage for maximum starting point of tuner takeover (RMS value)	input at pins 1, 2, 4 and 5; R_{TOP} = 0 Ω; I_{19} = 0.4 mA	50	100	–	mV
$V_{o,19}$	permissible output voltage	from external source; note 2	–	–	13.2	V
$V_{sat,19}$	saturation voltage	I_{19} = 1.5 mA	–	–	0.2	V
$\frac{\Delta V_{TOP,19}}{\Delta T}$	variation of takeover point by temperature	I_{19} = 0.4 mA	–	0.03	0.07	dB/K
$I_{19(sink)}$	sink current	see Fig.3				
		no tuner gain reduction; V_{19} = 13.2 V	–	–	5	μA
		maximum tuner gain reduction	1.5	2	2.6	mA
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20 to 80%	–	6	8	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AFC circuit (pin 23); see Fig.7 and note 16						
S_{USA}	control steepness $\Delta I_{23}/\Delta f$	f_0 = 45.75 MHz; see Fig.12 and note 17	0.6	0.91	1.2	μA/kHz
S_{EUR}		f_0 = 38.9 MHz; see Fig.12 and note 17	0.5	0.72	1.0	μA/kHz
$\frac{\Delta f_{IF}}{\Delta T}$	frequency variation by temperature	I_{AFC} = 0; note 5	–	–	±20	ppm/K
$V_{o,23}$	output voltage upper limit	see Fig.7	V_P – 0.6	V_P – 0.3	–	V
	output voltage lower limit	see Fig.7	–	0.3	0.6	V
$I_{o,23(source)}$	output source current		150	200	250	μA
$I_{o,23(sink)}$	output sink current		150	200	250	μA
$\Delta I_{23(p-p)}$	residual video modulation current (peak-to-peak value)	M, B/G and L standard	–	20	30	μA
Sound IF amplifier (pins 31 and 32); note 18						
$V_{i\ SIF(rms)}$	input signal voltage sensitivity (RMS value)	FM mode; –3 dB at intercarrier output pin 20	–	40	70	μV
		AM mode; –3 dB at AF output pin 12	–	80	110	μV
$V_{i\ max(rms)}$	maximum input signal voltage (RMS value)	FM mode; +1 dB at intercarrier output pin 20	40	80	–	mV
		AM mode; +1 dB at AF output pin 12	100	160	–	mV
G_{SIFcr}	SIF gain control range	FM and AM mode; see Fig.4	59	64	–	dB
$R_{i(diff)}$	differential input resistance	note 2	1.7	2.2	2.7	kΩ
$C_{i(diff)}$	differential input capacitance	note 2	1.2	1.7	2.5	pF
$V_{I(31,32)}$	DC input voltage		–	3.4	–	V
$\alpha_{SIF,VIF}$	crosstalk attenuation between SIF and VIF input	between pins 1, 2, 4 and 5 and pins 31 and 32; notes 2 and 3	50	–	–	dB
SIF-AGC detector (pin 8)						
I_8	charging current	FM mode	8	12	16	μA
		AM mode	0.8	1.2	1.6	μA
	discharging current	FM mode	8	12	16	μA
		normal mode AM	1	1.4	1.8	μA
		fast mode AM	60	85	110	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Single reference QSS intercarrier mixer (M and B/G standard; pin 20); note 18						
$V_{o(rms)}$	IF intercarrier level (RMS value)	SC_1; sound carrier 2 off	75	100	125	mV
B_{-3}	–3 dB intercarrier bandwidth	upper limit	7.5	9	–	MHz
$\alpha_{SC(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics	–	2	–	mV
$R_{o,20}$	output resistance	note 2	–	10	20	Ω
$V_{O,20}$	DC output voltage		–	2.0	–	V
$I_{int\ 20}$	DC internal bias current for emitter-follower		1.5	1.9	–	mA
$I_{20\ max(sink)}$	maximum AC and DC output sink current		1.1	1.5	–	mA
$I_{20\ max(source)}$	maximum AC and DC output source current		3.0	3.5	–	mA
Limiter amplifier (pin 17); note 19						
$V_{i\ FM(rms)}$	input signal voltage for lock-in (RMS value)		–	–	100	μV
$V_{i\ FM(rms)}$	input signal voltage (RMS value)	$\frac{S+N}{N}$ = 40 dB	–	300	400	μV
	allowed input signal voltage (RMS value)		200	–	–	mV
R_{17}	input resistance	note 2	480	600	720	Ω
V_{17}	DC input voltage		–	2.7	–	V
FM-PLL detector						
$f_{i\ FM(catch)}$	catching range of PLL	upper limit	7.0	–	–	MHz
		lower limit	–	–	4.0	MHz
$f_{i\ FM(hold)}$	holding range of PLL	upper limit	9.0	–	–	MHz
		lower limit	–	–	3.0	MHz
t_{acqu}	acquisition time		–	–	4	μs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM operation (M and B/G standard) (pin 12); note 19						
$V_{o\ AF12(rms)}$	AF output signal voltage (RMS value)	without de-emphasis; 25 kHz; see Fig.12 and note 20				
		R_x = 470 Ω	200	250	300	mV
		R_x = 0 Ω	400	500	600	mV
$V_{o\ AF12(cl)(rms)}$	AF output clipping signal voltage level (RMS value)	THD < 1.5%	1.3	1.4	–	V
Δf_{AF}	frequency deviation	THD < 1.5%; note 20	–	–	±53	kHz
ΔV_o	temperature drift of AF output signal voltage		–	3	7	10^{-3} dB/K
V_{14}	DC voltage at decoupling capacitor	voltage dependent on VCO frequency; note 21	1.2	–	3.0	V
R_{12}	output resistance	note 2	–	–	100	Ω
V_{12}	DC output voltage	tracked with supply voltage	–	$\frac{1}{2}V_P$	–	V
$I_{12(max)(sink)}$	maximum AC and DC output sink current		–	–	1.1	mA
$I_{12(max)(source)}$	maximum AC and DC output source current		–	–	1.1	mA
B_{-3}	–3 dB AF bandwidth	without de-emphasis	100	125	–	kHz
THD	total harmonic distortion		–	0.15	0.5	%
S/N (W)	weighted signal-to-noise ratio	FM-PLL only; with 75 µs de-emphasis; 25 kHz; *"CCIR 468-4"*	55	60	–	dB
$\alpha_{c(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics	–	–	75	mV
α_{AM}	AM suppression	75 µs de-emphasis; AM: f = 1 kHz; m = 0.3 referenced to 25 kHz	45	50	–	dB
α_{12}	mute attenuation of AF signal		68	73	–	dB
$I_{17(mute)}$	current output from pin 17	AF signal muted	200	300	600	µA
ΔV_{12}	DC jump voltage of AF output terminal for switching AF output to mute state and vice versa	FM-PLL in lock mode	–	±50	±150	mV
PSRR	power supply ripple rejection at pin 12	M standard; see Fig.9	26	30	–	dB
		B/G standard; see Fig.9	20	24	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Single reference QSS AF performance for FM operation (M standard); see Table 1 and notes 20 and 22 to 24; sound attenuation of VIF SAW filter: minimum 33 dB						
S/N (W)	weighted signal-to-noise ratio	PC/SC ratio at pins 1 and 2; 25 kHz FM deviation; 75 µs de-emphasis; *"CCIR 468-4"*	40	–	–	dB
		black picture	51	56	–	dB
		white picture	50	53	–	dB
		colour bar	48	51	–	dB
Single reference QSS AF performance for FM operation (B/G standard); see Table 1 and notes 20 and 22 to 24; sound attenuation of VIF filter: minimum 27 dB						
S/N (W)	weighted signal-to-noise ratio (SC_1/SC_2)	PC/SC ratio at pins 1 and 2; 27 kHz; *"CCIR 468-4"*; 50 µs de-emphasis	40	–	–	dB
		black picture	53/48	58/55	–	dB
		white picture	52/46	55/53	–	dB
		6 kHz sine wave (black to white modulation)	44/42	48/46	–	dB
AM operation (L standard; pin 12); note 25						
$V_{o\ AF\ 12(rms)}$	AF output signal voltage (RMS value)	54% modulation	400	500	600	mV
THD	total harmonic distortion	54% modulation	–	0.5	1.0	%
B_{-3}	−3 dB AF bandwidth		100	125	–	kHz
S/N (W)	weighted signal-to-noise ratio	*"CCIR 468-4"*	47	53	–	dB
V_{12}	DC potential voltage	tracked with supply voltage	–	$\frac{1}{2}V_P$	–	V
PSRR	power supply ripple rejection	see Fig.9	22	25	–	dB
Standard switch (pin 9); see also Table 2						
V_9	DC potential for settings					
V_{IH}	HIGH level input voltage		1.3	–	V_P	V
V_{IL}	LOW level input voltage		0	–	0.8	V
I_{IL}	LOW level input current	V_9 = 0 V	85	110	135	µA
VIF input/DVB switch (pin 30); see also Table 2						
V_{30}	DC potential for settings					
V_{IH}	HIGH level input voltage		1.3	–	V_P	V
V_{IL}	LOW level input voltage		0	–	0.8	V
I_{IL}	LOW level input current	V_{30} = 0 V	180	230	280	µA
VCO adjust (pin 11)						
V_{11}	DC potential for VCO frequency adjust		0	1	2	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIF amplifier (measured at f_{IF} = 43.75 MHz; DVB mode)						
$V_{4-5(rms)}$	input sensitivity (RMS value)	–1 dB α_{AM} signal at output	–	200	–	μV
$V_{4-5(rms)}$	maximum input signal (RMS value)	+1 dB α_{AM} signal at output	–	200	–	mV
ΔG	total gain control IF amplifier		52	58	–	dB
	tilt for Δf ±3 MHz	f_s = 6.9 MHz; 40 dB gain	–	0.5	1	dB
$R_{4-5(diff)}$	input resistance (differential)	note 2	–	2.2	–	kΩ
$C_{4-5(diff)}$	input capacitance (differential)	note 2	–	1.7	–	pF
DVB mixer and VCO						
f_{VCO}	maximum oscillator frequency	$2(f_{IF} + f_s)$	125	130	–	MHz
$V_{0\ ref(rms)}$	oscillator voltage swing between pins 24 and 25 (RMS value)		–	60	–	mV
$\Delta\varphi_{SSB}$	VCO phase noise at f = 100 kHz	free-running	103	107	–	dBc/Hz
V_{16}	VCO control range	see Figs 10 and 11	0	–	V_P	V
$R_{i,16}$	VCO control input resistance		50	63	76	kΩ
S_{VCO}	control steepness $\Delta f_s/\Delta V_{16}$	see Figs 10 and 11				
		DVB (USA)	–	0.29	–	MHz/V
		DVB (EUROPE)	–	0.40	–	MHz/V
DVB output buffer						
$V_{O\ DVB(p-p)}$	DVB output signal (QAM) (peak-to-peak value)		1.8	2.1	2.4	V
$I_{int\ 18}$	DC internal bias current for emitter-follower		1.9	2.3	2.7	mA
$I_{18\ max(sink)}$	maximum AC and DC output sink current		1.5	–	–	mA
$I_{18\ max(source)}$	maximum AC and DC output source current		2.0	–	–	mA
DVB AGC detector						
t_{resp}	response to an increasing amplitude step in the IF input signal		–	0.25	0.1	ms/dB
	response to a decreasing amplitude step in the IF input signal		–	0.25	–	ms/dB
I_{28}	charging current		–	200	–	μA
	discharging current		–	200	–	μA
V_{15}	AGC adjust input voltage range		1	2.5	4.5	V
$R_{i,15}$	AGC adjust input resistance		8	10	12	kΩ
S_{adj}	AGC adjust steepness	2 V < V_{15} < 3 V	–	–5	–	dB/V
V_{13}	external AGC voltage for DVB	see Fig.3	1	–	4.5	V
$R_{i,13}$	external AGC input resistance		40	–	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AFC circuit (DVB mode)						
S_{US}	control steepness $\Delta I_{23}/\Delta f$	f_0 = 48.75 MHz; see Fig.12 and note 17	0.7	0.98	1.3	μA/kHz
S_{EU}		f_0 = 43.0 MHz; see Fig.12 and note 17	0.45	0.70	0.95	μA/kHz
DVB output signal (IF input to DVB output)						
$V_{18(p-p)}$	output voltage (peak-to-peak value)	C_L < 15 pF; R_L > 5 kΩ; with internal AGC	1.8	2.1	2.4	V
V_{18DC}	DC voltage		–	2.5	–	V
B	–1 dB bandwidth	C_L < 15 pF; R_L > 5 kΩ	11	12	–	MHz
	–3 dB bandwidth		–	17	–	MHz
$\alpha_{C(DVB)}$	fundamental input signal and IF harmonics		35	40	–	dB
α_H	suppression of in-band harmonics	2.0 V (p-p) output voltage	30	35	–	dB

Notes to the characteristics

1. Values of video and sound parameters are decreased at V_P = 4.5 V.
2. This parameter is not tested during production and is only given as application information for designing the television receiver.
3. Source impedance: 2.3 kΩ in parallel to 12 pF (SAW filter); f_{IF} = 45 MHz.
4. Loop filter 330 Ω/220 nF; loop bandwidth for M standard: BL ≈ 70 kHz (natural frequency f_n ≈ 12 kHz; damping factor d ≈ 2.9; loop bandwidth for B/G and L standard: BL ≈ 80 kHz (natural frequency f_n ≈ 13 kHz; damping factor d ≈ 3.2; calculated with sync level within gain control range). Resonance circuit of VCO: Q_0 > 50; C_{ext} and C_{int} see Fig.12.
5. Temperature coefficient of external LC-circuit is equal to zero.
6. $V_{i\ IF}$ = 10 mV RMS; Δf = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
7. $V_{i\ IF}$ signal for nominal video signal.
8. Offset current measured between pin 7 and half of supply voltage (V_P = 2.5 V) under the following conditions: no input signal at VIF input (pins 1, 2, 4 and 5) and VIF amplifier gain at minimum (V_{28} = V_P). Due to sample-and-hold mode of the FPLL in L standard, the leakage current of the loop filter capacitor (C = 220 nF) should not exceed 500 nA.
9. Measurements taken with SAW filter M3951M and M9352M (Siemens, M standard); frequency range = 10 kHz to 5 MHz. Sound carrier ON; PC/SC ratio 7 dB (transmitter); modulation VSB.
10. The 7 dB buffer gain accounts for 1 dB loss in the sound trap. Buffer output signal is typical 2 V (p-p), in event of CVBS video amplifier output typical 1 V (p-p). If no sound trap is applied a 330 Ω resistor must be connected from output to input (from pin 21 to pin 22).
11. The leakage current of the AGC capacitor should not exceed 1 μA at M and B/G standard respectively 10 nA current at L standard. Larger currents will increase the tilt.
12. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 10). B = 5 MHz weighted in accordance with *"CCIR 567"*.

13. The intermodulation figures are defined:

$$\alpha_{0.92} = 20 \log\left(\frac{V_0 \text{ at } 3.58\text{ MHz}}{V_0 \text{ at } 0.92\text{ MHz}}\right) + 3.6\,\text{dB}$$; $\alpha_{0.92}$ value at 0.92 MHz referenced to black/white signal;

$$\alpha_{2.76} = 20 \log\left(\frac{V_0 \text{ at } 3.58\text{ MHz}}{V_0 \text{ at } 2.76\text{ MHz}}\right)$$; $\alpha_{2.76}$ value at 2.76 MHz referenced to colour carrier.

14. Sound carrier ON; SIF SAW filter L9453; f_{video} = 10 kHz to 10 MHz.
15. Response speed valid for a VIF input level range of 200 μV up to 70 mV.
16. To match the AFC output signal to different tuning systems a current source output is provided. The test circuit is given in Fig.7. The AFC-steepness can be changed by the resistors at pin 23.
17. Depending on the ratio $\Delta C/C_0$ of the LC resonant circuit of VCO ($Q_0 > 50$; $C_0 = C_{int} + C_{ext}$; see Fig.12).
18. The intercarrier mode can be activated by connecting the SIF input pins 31 and 32 to GND (only for negative modulation standard BG/M). In this event the intercarrier level depends on the sound shelf of VIF SAW filter and the transmitter PC/SC ratio.
19. Input level for second IF from an external generator with 50 Ω source impedance. AC-coupled with 10 nF capacitor, f_{mod} = 400 Hz, 25 kHz (50% FM deviation) of audio references. A VIF/SIF input signal is not permitted. Pins 8 and 28 have to be connected to positive supply voltage for minimum IF gain. S/N and THD measurements are taken at 75 μs de-emphasis. The FM demodulator steepness $\Delta V_{o\,AF}/\Delta f_{AF}$ is negative.
20. Measured with an FM deviation of 25 kHz the typical AF output signal is 500 mV RMS (R_x = 0 Ω; see Fig.12). By using R_x = 470 Ω the AF output signal is attenuated by 6 dB (250 mV RMS). For handling an FM deviation of more than 53 kHz the AF output signal has to be reduced by using R_x in order to avoid clipping (THD < 1.5%). For an FM deviation up to 100 kHz an attenuation of 6 dB is recommended with R_x = 470 Ω.
21. The leakage current of the decoupling capacitor (2.2 μF) should not exceed 1 μA.
22. For all S/N measurements the used vision IF modulator has to meet the following specifications:
    Incidental phase modulation for black-to-white jump less than 0.5 degrees;
    QSS AF performance, measured with the television-demodulator AMF2 (audio output, weighted S/N ratio) better than 60 dB (deviation 25 kHz) for 6 kHz sine wave black-to-white video modulation.
23. The PC/SC ratio at pins 1 and 2 is calculated as the addition of TV transmitter PC/SC ratio and SAW filter PC/SC ratio. This PC/SC ratio is necessary to achieve the S/N(W) values as noted. A different PC/SC ratio will change these values.
24. Measurements for M standard with SAW filter M3951M (Siemens) for vision IF (suppressed sound carrier) and M9352M (Siemens) for sound IF (suppressed picture carrier). Input level $V_{i\,SIF}$ = 10 mV RMS, 25 kHz FM deviation.

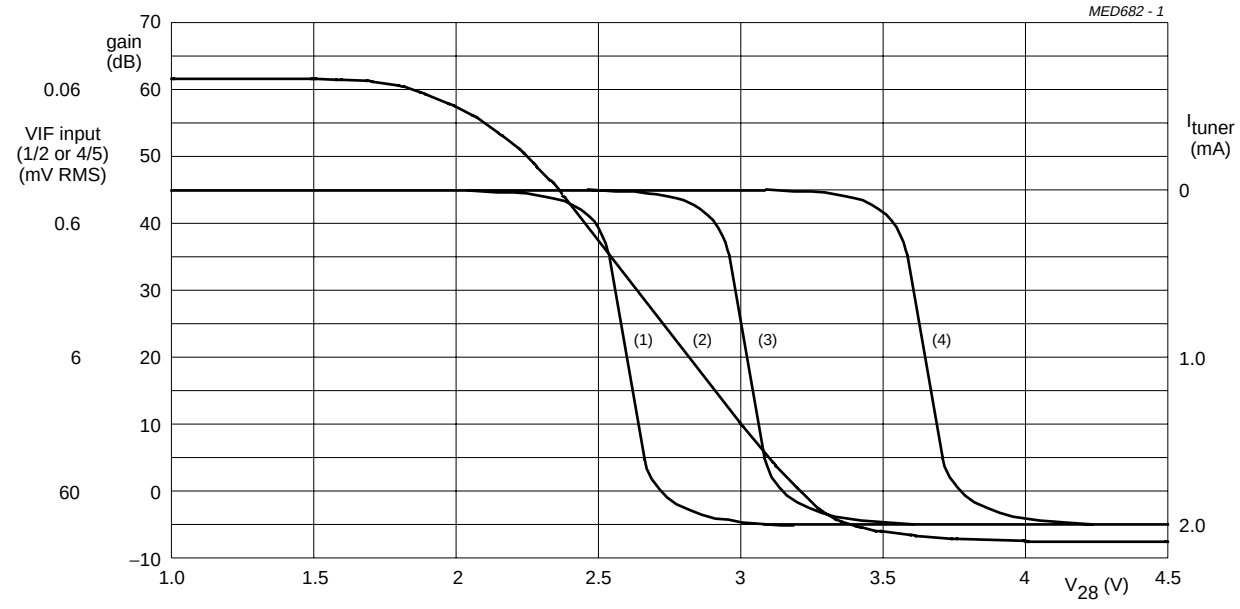
    Measurements for B/G standard with SAW filter G3962 (Siemens) for vision IF (suppressed sound carrier) and G9350 (Siemens) for sound IF (suppressed picture carrier). Input level $V_{i\,SIF}$ = 10 mV RMS, 27 kHz (54% FM deviation).
25. Measurements taken with SAW filter L9453 (Siemens) for AM sound IF (suppressed picture carrier).

Table 1 Input frequencies and carrier ratios

DESCRIPTION	SYMBOL	B/G STANDARD	M STANDARD	L STANDARD	DVB (EU)	DVB (US)	UNIT
Symbol frequency	f_{IF}/f_s	–	–	–	36.15/6.9	43.75/5.0	MHz
Picture carrier	f_{PC}	38.9	45.75	38.9	–	–	MHz
Sound carrier	f_{SC1}	33.4	41.25	32.4	–	–	MHz
	f_{SC2}	33.158	–	–	–	–	MHz
Picture-to-sound carrier ratio	SC_1	13	7	10	–	–	dB
	SC_2	20	–	–	–	–	dB

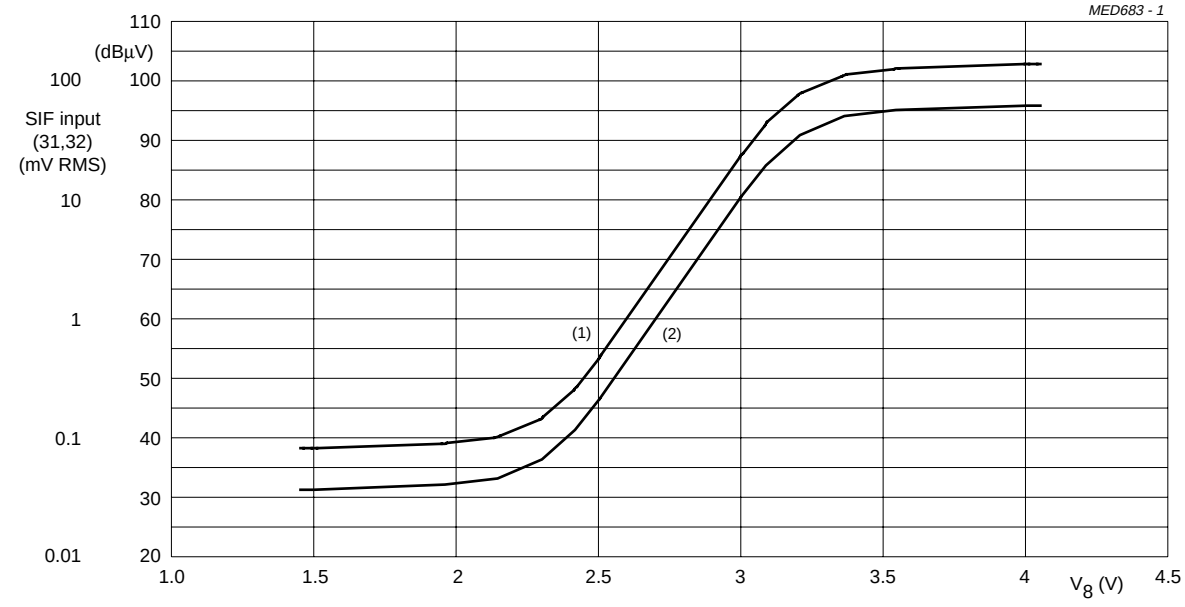
Table 2 Switch logic

STANDARD	INPUT SWITCH	STANDARD SWITCH	MODULATION MODE	AGC	VCO CONTROL	IF INPUT	AF	VIDEO OUTPUT	
								M, B/G, L	DVB
DVB	0	0	digital	external	external	B	mute	off	on
	0	1	digital	internal	external	B	mute	off	on
Standard M, B/G and L	1	0	positive	internal	PLL	A	AM	on	off
	1	1	negative	internal	PLL	A	FM	on	off



(1) I_{tuner}; R_{TOP} = 22 kΩ.
(2) Gain.
(3) I_{tuner}; R_{TOP} = 11 kΩ.
(4) I_{tuner}; R_{TOP} = 0 Ω.

Fig.3 Typical VIF and tuner AGC characteristic.



(1) AM mode.
(2) FM mode.

Fig.4 Typical SIF AGC characteristic.

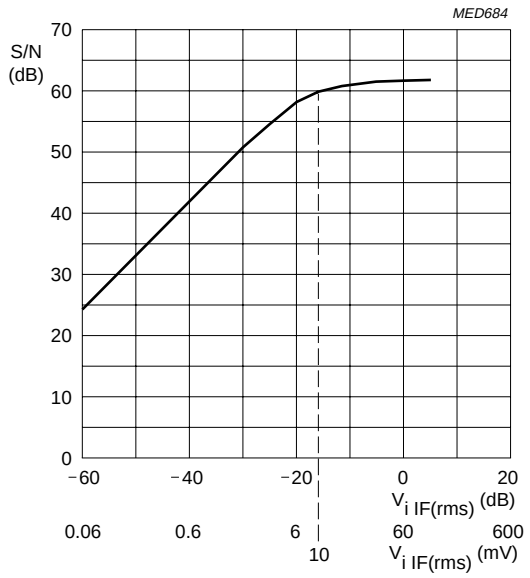
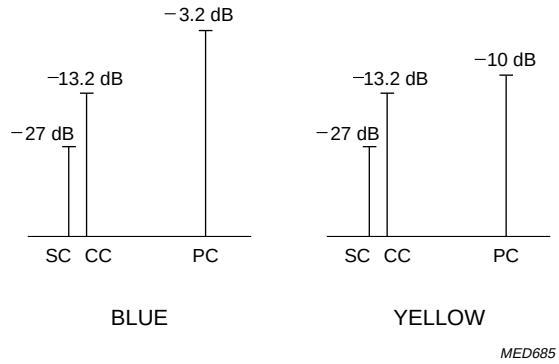


Fig.5 Typical signal-to-noise ratio as a function of IF input voltage.



SC = sound carrier, with respect to sync level.
CC = chrominance carrier, with respect to sync level.
PC = picture carrier, with respect to sync level.
The sound carrier levels are taking into account a sound shelf attenuation of 20 dB (SAW filter G1962).

Fig.6 Input signal conditions.

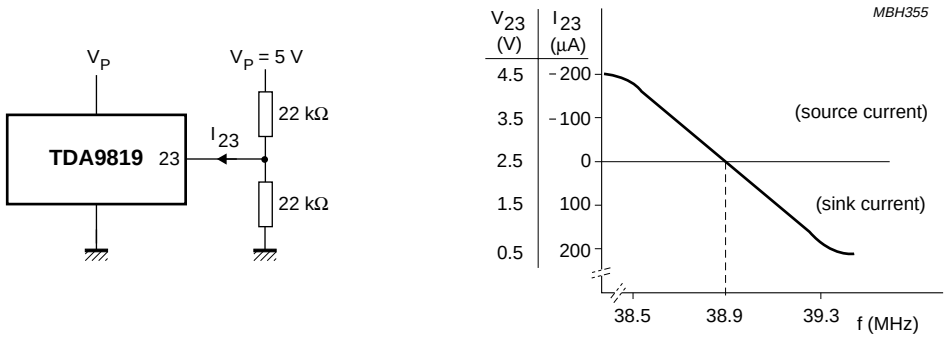


Fig.7 Measurement conditions and typical AFC characteristic.

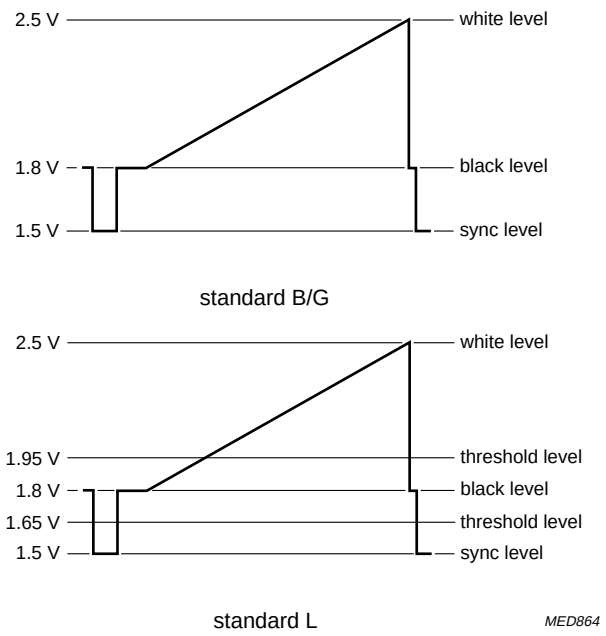


Fig.8 Typical video signal levels on output pin 21 (sound carrier **off**).

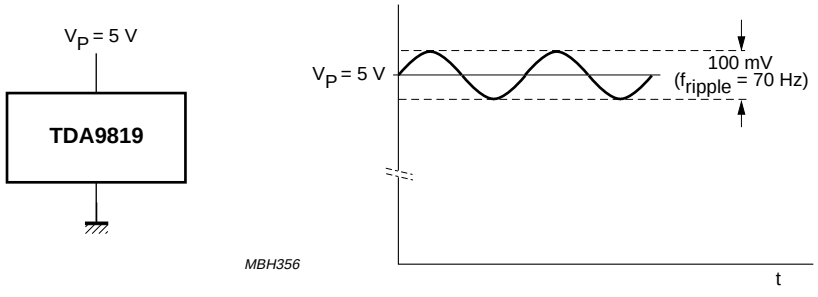
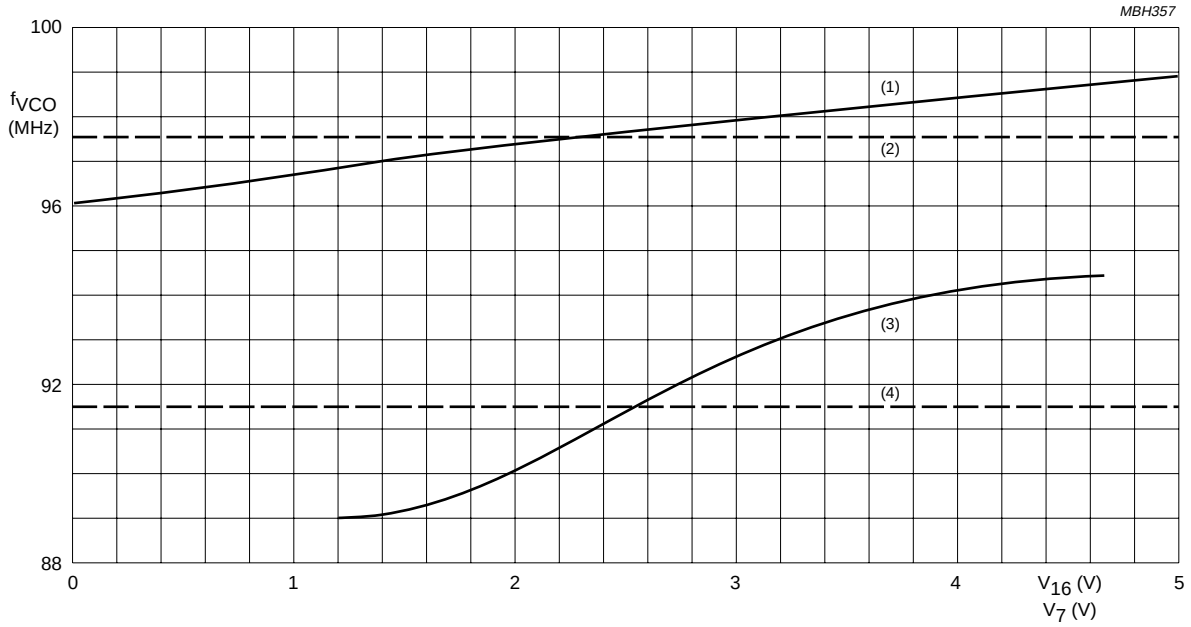


Fig.9 Ripple rejection condition.



L = 115 nH and C = 15 pF.

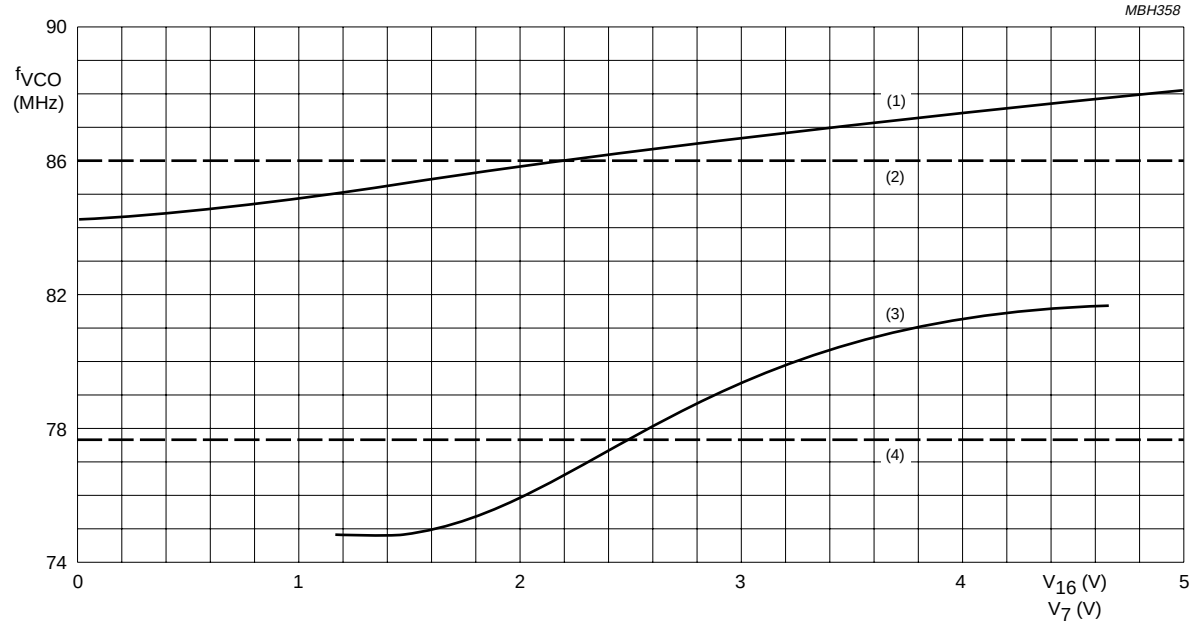
(1) DVB.

(2) f_0 = 97.5 MHz.

(3) M standard.

(4) f_0 = 91.5 MHz.

Fig.10 VCO control characteristic for standard M and DVB (USA).



L = 248 nH and C = 5.6 pF.

(1) DVB.

(2) f_0 = 86.0 MHz.

(3) BG/L standard.

(4) f_0 = 77.8 MHz.

Fig.11 VCO control characteristic for standard BG/L and DVB (EUROPE).

TEST CIRCUIT

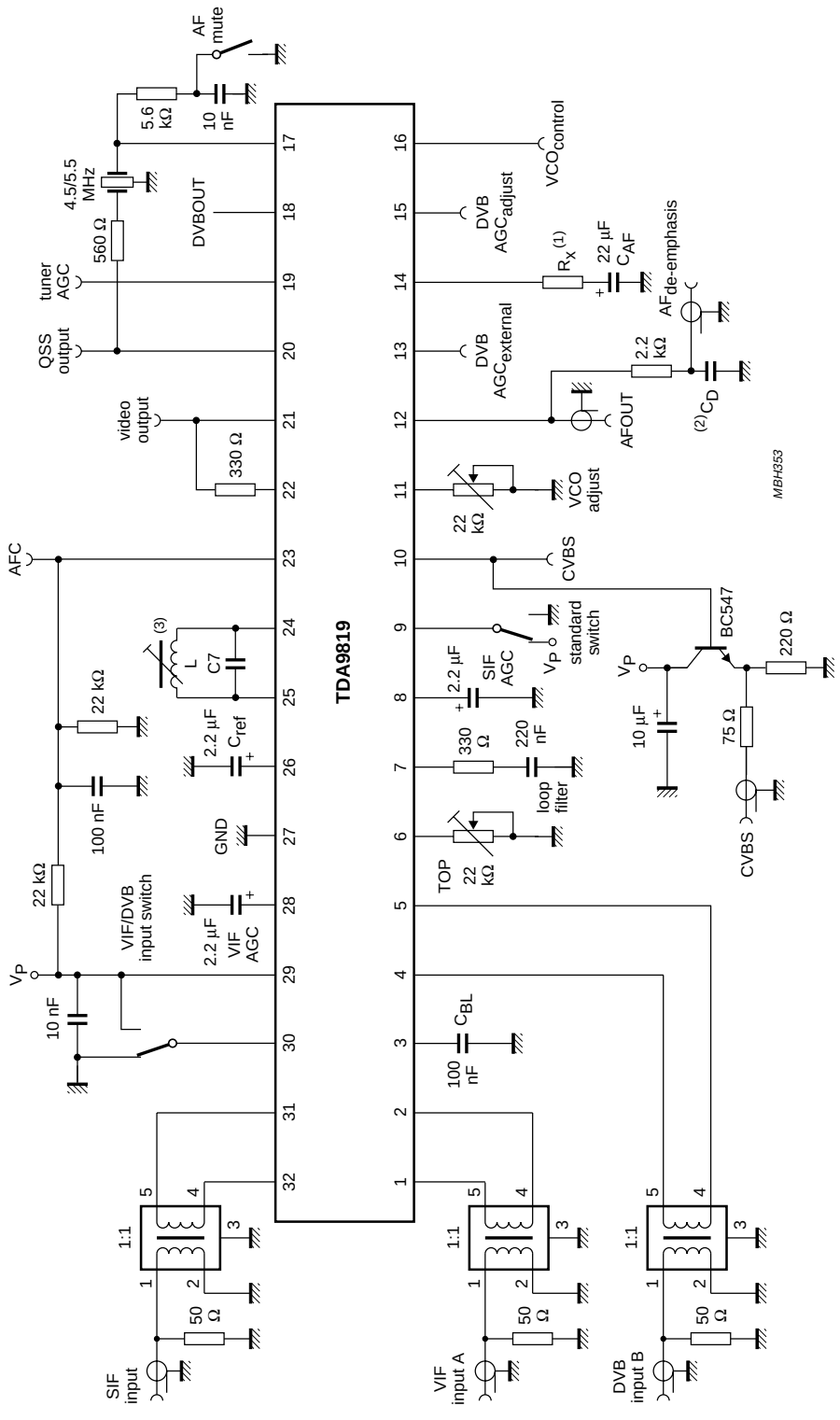
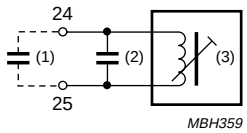
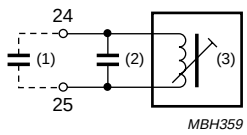


Fig.12 Test circuit.

(1) See note 20 in Chapter "Characteristics".
(2) C_D = 22 nF for 50 µs de-emphasis; C_D = 33 nF for 75 µs de-emphasis.
(3) See Table 3.

Table 3 Test circuit values

PARAMETER	EUROPE	USA
IF frequency	36.15/38.9 MHz	43.75/45.75 MHz
VCO frequency	86.0/77.8 MHz	97.5/91.5 MHz
Oscillator circuit	 (1) C(VCO) = 8.2/11.3 pF. (2) C7 = 5.6 pF. (3) L = 248 nH.	 (1) C(VCO) = 8.2/11.3 pF. (2) C7 = 15 pF. (3) L = 115 nH.
Toko coil	5KM 369SNS - 2010Z	5KM 369SNS - 1647Z
Philips ceramic capacitor	2222 632 39478	2222 632 33129

INTERNAL PIN CONFIGURATIONS

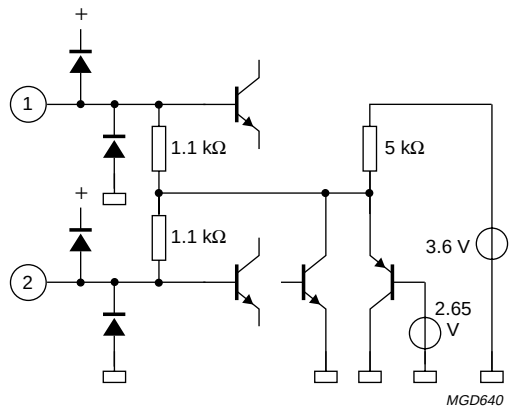


Fig.13 Pin 1; $V_{i\ VIF1}$ and pin 2; $V_{i\ VIF2}$.

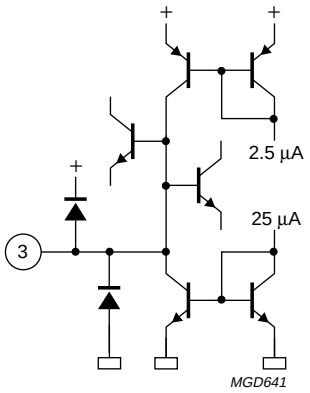


Fig.14 Pin 3; C_{BL}.

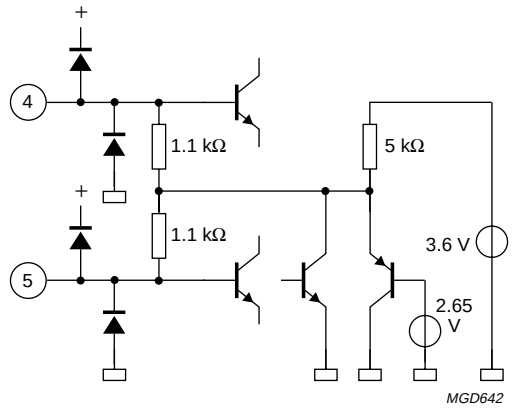


Fig.15 Pin 4; $V_{i\ VIF3}$ and pin 5; $V_{i\ VIF4}$.

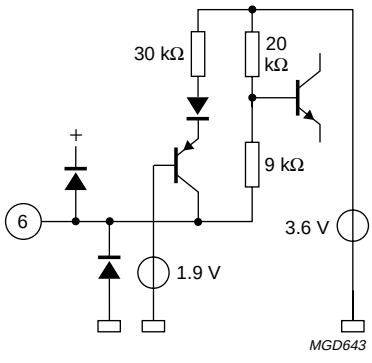


Fig.16 Pin 6; TADJ.

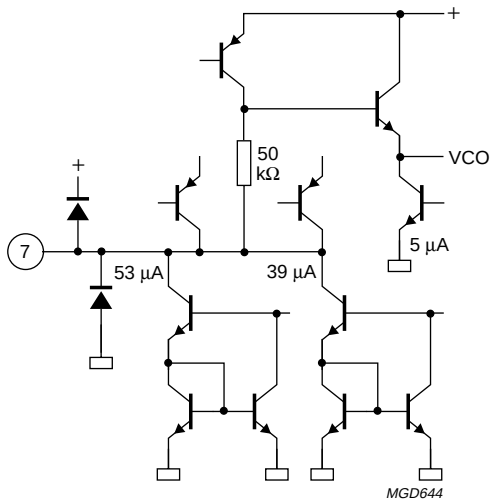


Fig.17 Pin 7; T_{PLL}.

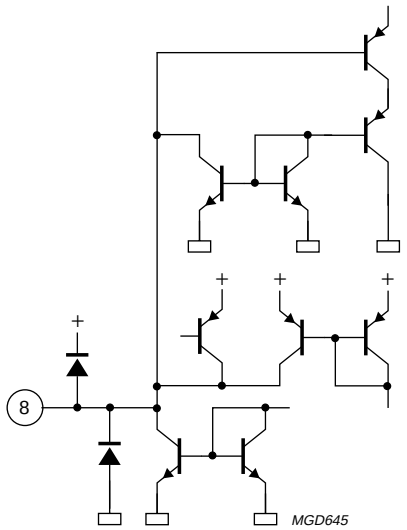


Fig.18 Pin 8; C_{SAGC}.

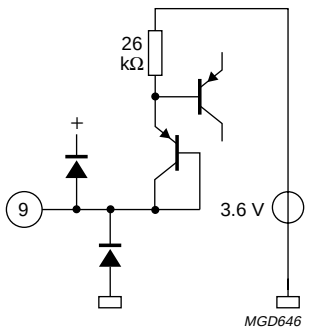


Fig.19 Pin 9; STD.

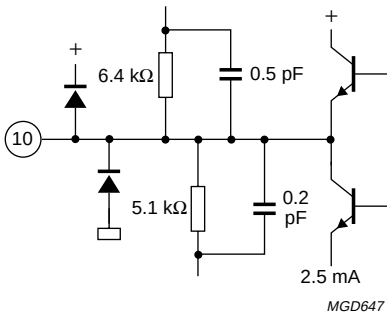


Fig.20 Pin 10; $V_{o\ CVBS}$.

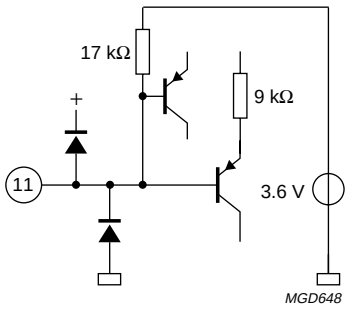


Fig.21 Pin 11; VCOADJ.

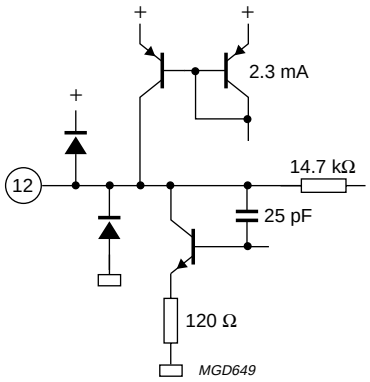


Fig.22 Pin 12; $V_{o\ AF}$.

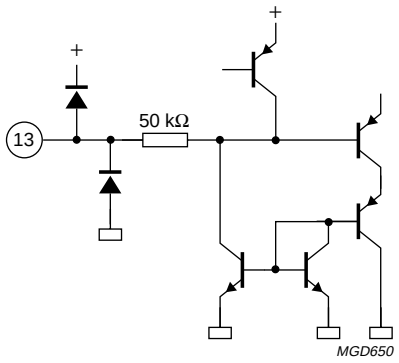


Fig.23 Pin 13; $V_{AGC(ext)}$.

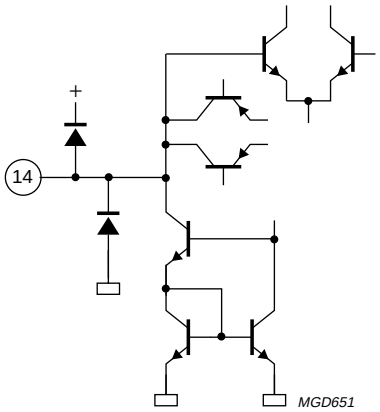


Fig.24 Pin 14; $C_{AF.}$

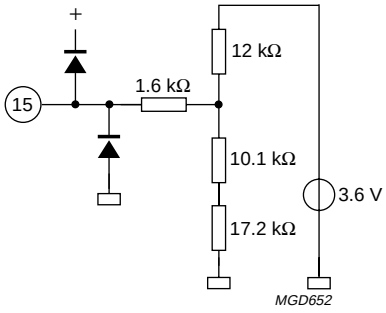


Fig.25 Pin 15; AGCADJ.

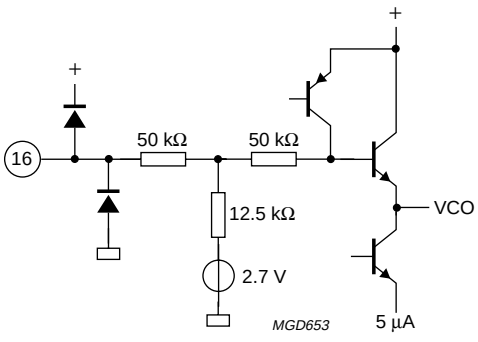


Fig.26 Pin 16; $V_{VCO(ext)}$.

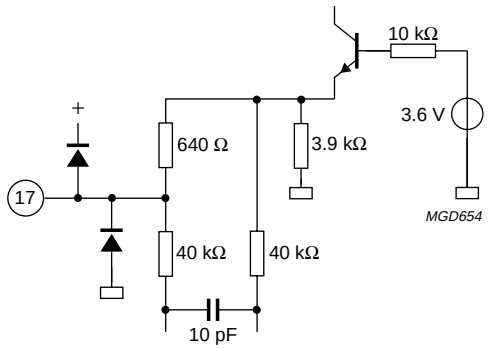


Fig.27 Pin 17; $V_{i\,FM}$.

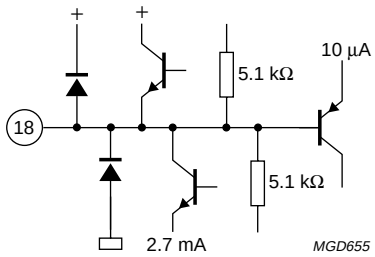


Fig.28 Pin 18; DVB.

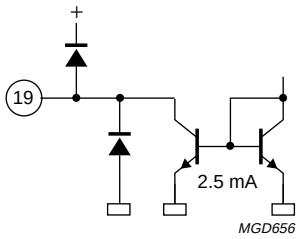


Fig.29 Pin 19; TAGC.

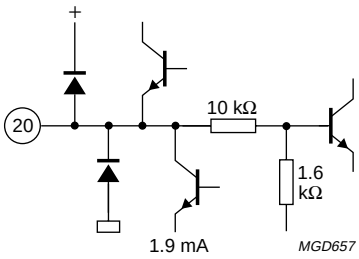


Fig.30 Pin 20; $V_{o\,QSS}$.

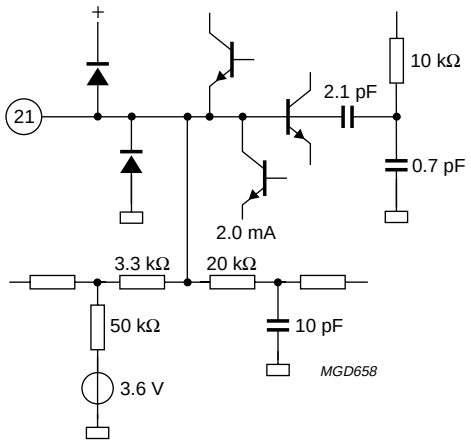


Fig.31 Pin 21; $V_{o(vid)}$.

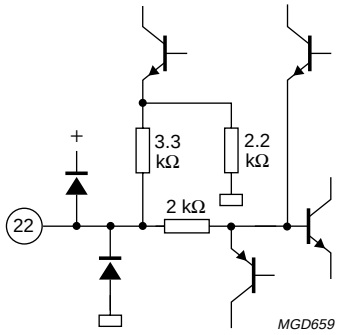


Fig.32 Pin 22; $V_{i(vid)}$.

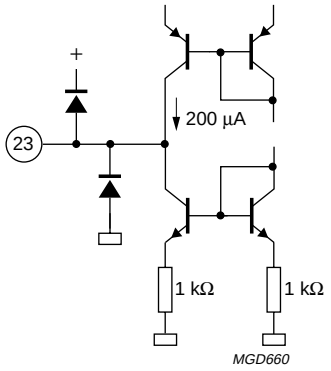


Fig.33 Pin 23; AFC.

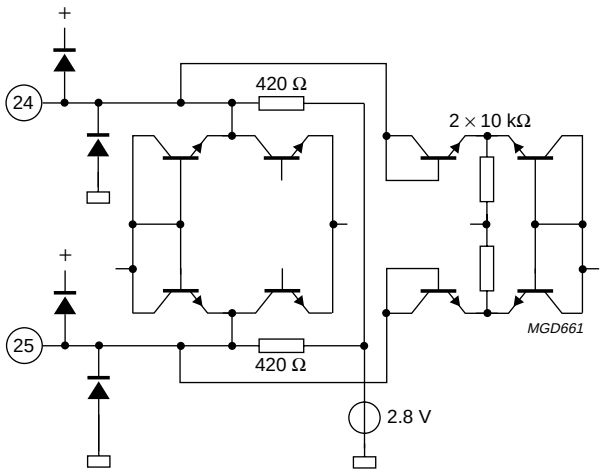


Fig.34 Pin 24; VCO1 and pin 25; VCO2.

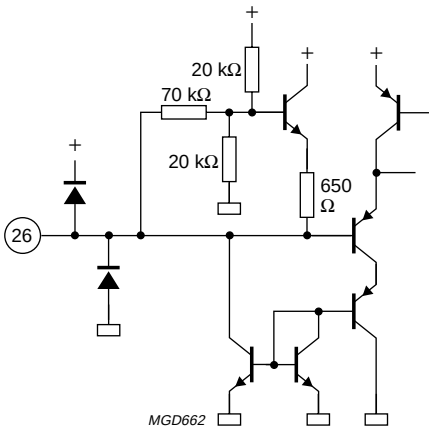


Fig.35 Pin 26; C_{ref}.

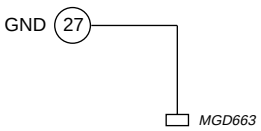


Fig.36 Pin 27; GND.

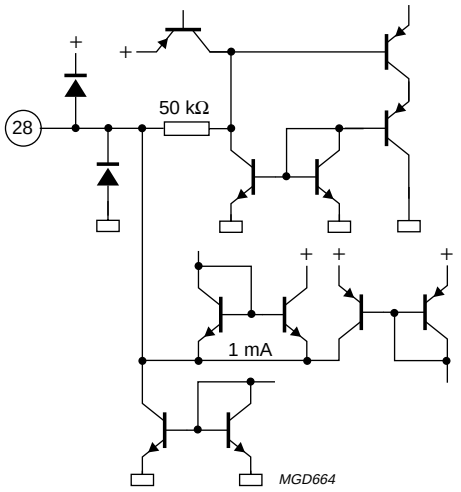


Fig.37 Pin 28; C_{VAGC}.

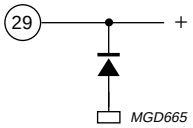


Fig.38 Pin 29; V_P.

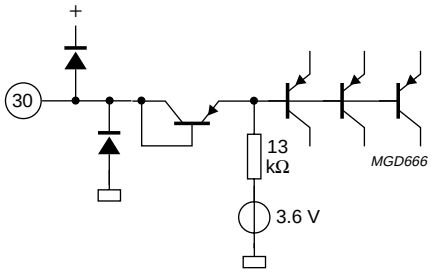


Fig.39 Pin 30; INSWI.

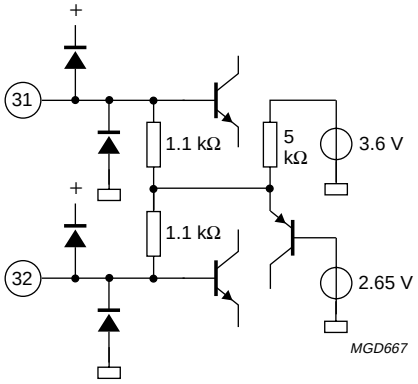
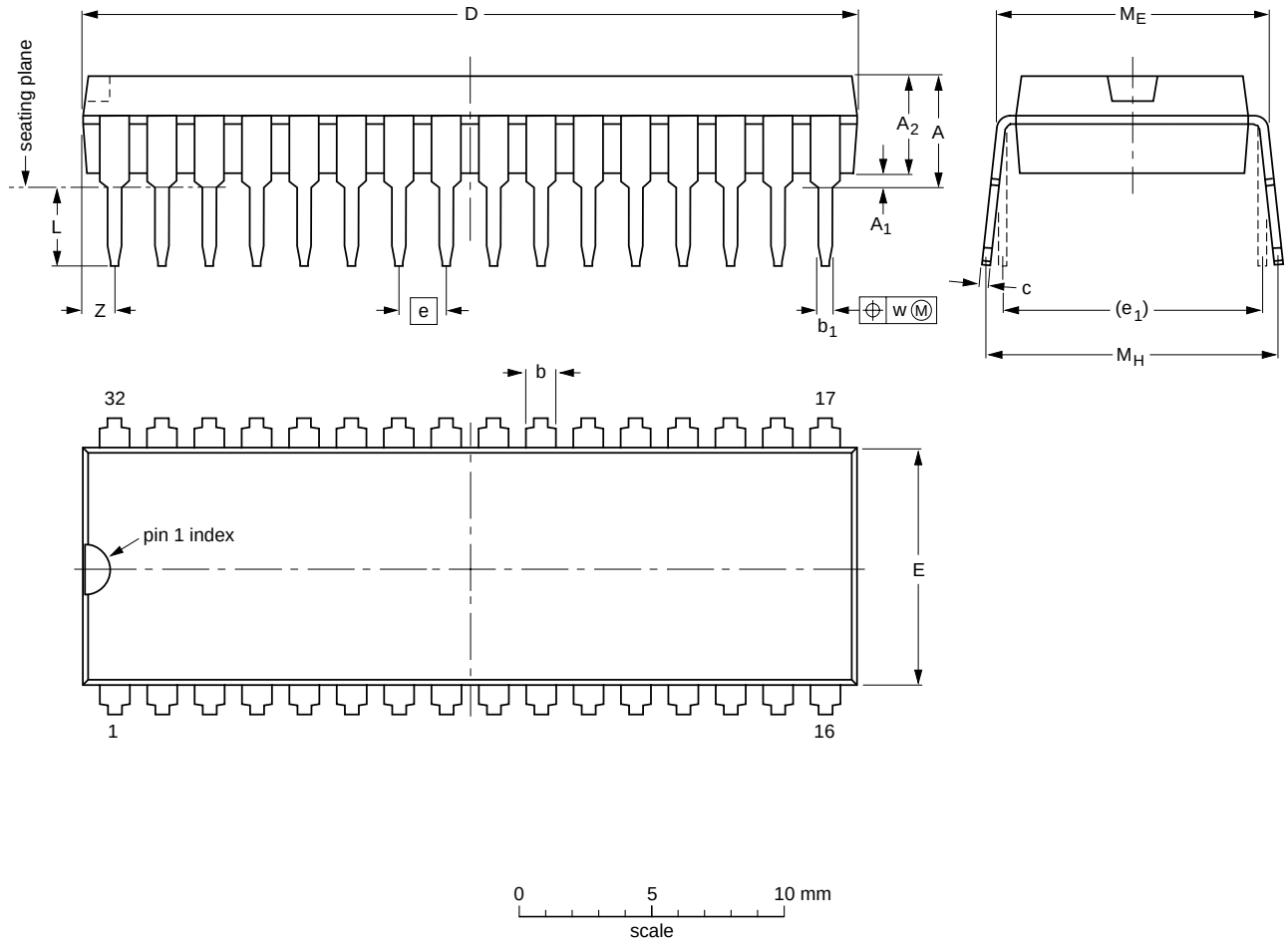


Fig.40 Pin 31; $V_{i\ SIF1}$ and pin 32; $V_{i\ SIF2}$.

PACKAGE OUTLINE

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil) **SOT232-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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